I. PLEASE AMEND THE APPLICATION AS FOLLOWS:

AMENDMENTS TO THE CLAIMS:

1. (Original) A synchronous dynamic memory operating in synchronized with an external clock, comprising:

a clock input buffer receiving said external clock and outputting an internal clock;

a command input buffer receiving commands in synchronization with said internal clock;

an address input buffer receiving addresses in synchronization with said internal clock; and

a data input buffer receiving data in synchronization with said internal clock;

wherein said clock input buffer supplies said internal clock to said command, address, and data input buffers in normal operation mode, and wherein said clock input buffer supplies said internal clock to said command input buffer and stops supply of said internal clock to said address input buffer or data input buffer in data hold mode.

2. (Original) The synchronous dynamic memory according to claim 1, further comprising:

a first clock supply line that supplies said internal clock to said command input buffer; and

a second clock supply line that supplies said internal clock to said address input buffer or said data input buffer;

wherein said clock input buffer drives said first and second clock supply lines in normal operation mode, and said clock input buffer drives said first clock supply line and stops driving said second clock supply line in said data hold mode.

3. (Original) The synchronous dynamic memory according to claim 2, wherein said first clock supply line is shorter than said second clock supply line.

4. (Original) The synchronous dynamic memory according to claim 1, wherein said clock input buffer receives a clock enable signal that distinguishes between normal operation mode and power down mode, and said data hold mode includes this power down mode.

5. (Original) A synchronous dynamic memory operating in synchronized with an external clock, comprising:

a clock input buffer receiving the external clock and outputting an internal clock;

a command input buffer receiving commands in synchronization with said internal clock;

an address input buffer receiving addresses in synchronization with said internal clock; and

a data input buffer receiving data in synchronization with said internal clock;

wherein said clock input buffer supplies the internal clock to said command, address, and data input buffers in normal operation mode, supplies the internal clock to said command input buffer and stops supplying a clock to said address input buffer or

said data input buffer in data hold mode without being accessed for read/write, and stops supplying the internal clock internally in power down mode.

6. (Original) The synchronous dynamic memory according to claim 5, comprising:

a first clock supply line that supplies said internal clock to said command input buffer; and

a second clock supply line that supplies said internal clock to said address input buffer or said data input buffer;

wherein said clock input buffer drives said first and second clock supply lines in normal operation mode, drives said first clock supply line and stops driving said second clock supply line in said data hold mode, and stops driving said first and second clock supply lines in power down mode.

7. (Original) The synchronous dynamic memory according to claim 6, wherein said first clock supply line is shorter than said second clock supply line.

8. (Original) The synchronous dynamic memory according to claim 5, wherein said clock input buffer inputs a first signal that distinguishes between normal operation mode and power down mode and a second signal that prompts said data hold mode.

9. (Original) An LSI, wherein the synchronous dynamic memory described in any one of claims 1 through 8 is embedded on one chip with a processing circuit macro that implements a prescribed processing.

10. (Previously Presented) The LSI according to claim 5, further comprising a memory controller that controls said synchronous dynamic memory.

11. (Original) A synchronous dynamic memory operating in synchronized with an external clock, comprising:

a clock input buffer receiving the external clock and outputting an internal clock;

a command input buffer receiving commands in synchronization with said internal clock;

an address input buffer receiving addresses in synchronization with said internal clock; and

a data input buffer receiving data in synchronization with said internal clock;

wherein a signal that distinguishes between a first operation mode and a second operation mode is supplied to said clock input buffer, and

wherein said clock input buffer supplies said internal clock to each of said command, address, and data input buffers in said first operation mode, and supplies said internal clock to said command input buffer and stops supplying the internal clock to said address input buffer or said data input buffer in said second operation mode.

12. (Canceled).

13. (Currently Amended) [[The]] A semiconductor integrated circuit comprising:

a clock buffer for generating an internal clock signal;

an input buffer that fetches an input signal in synchronization with said internal clock signal provided from [[the]] said clock buffer; and

a clock buffer controller ~~that monitors if there is a change in said input signal and activates said clock buffer, only when detecting the change in said input signal, so that the clock buffer generates the internal clock signal and provides the~~ that, upon detecting a change in said input signal, activates said clock buffer to generate said internal clock signal and to provide said internal clock signal to said input buffer.

14. (Currently Amended) [[A]] The semiconductor integrated circuit according to claim 13, ~~comprising:~~

~~a clock buffer for generating an internal clock signal;~~

~~an input buffer that fetches an input signal in synchronization with said internal clock signal provided from the clock buffer; and~~

wherein [[a]] said clock buffer controller [[that]] compares said input signal with an internal signal output from said input buffer ~~and activates said clock buffer when~~ to detect the change in said input signal ~~differs from said internal signal, so that the clock buffer generates the internal clock signal and provides the internal clock signal to said input buffer~~.

15. (Currently Amended) A semiconductor integrated circuit comprising:

a clock buffer for generating an internal clock signal;

a plurality of input buffers that fetches input signals in synchronization with said internal clock signal generated by said clock buffer; and

a clock buffer controller ~~that monitors if there is a change in said input signals respectively supplied into said plurality of input buffers, and activates said clock buffer when detecting the change in said input signal supplied into at least one of said input buffers~~ that, upon detecting a change in at least one of said input signals, activates said clock buffer to generate said internal clock signal and to provide said internal clock signal to said plurality of input buffers.

16. (Currently Amended) A semiconductor integrated circuit comprising:

a clock buffer for generating an internal clock signal;

a plurality of input buffers that fetches input signals in synchronization with said internal clock signal generated by said clock buffer; and

a plurality of [[the]] clock buffer controllers ~~being provided corresponding to~~ each corresponding to one of said input buffers~~, each of said clock buffer controllers including a signal change monitoring circuit that activates said clock buffer when there is a change in said input signal input into said corresponding input buffer~~ that, upon detecting a change in said input signal supplied to each corresponding input buffer, activates said clock buffer to generate said internal clock signal and to provide said internal clock signal to said plurality of input buffers.

17. (Currently Amended) The semiconductor integrated circuit according to claim 16, wherein ~~said signal change monitoring circuit includes~~ each of said clock buffer controllers includes a comparative circuit that compares said input signal with a corresponding internal signal output from [[said]] each corresponding input buffer, and

wherein said ~~clock buffer controller~~ semiconductor integrated circuit further ~~includes~~ comprises a logic circuit that logically synthesizes signals output from a plurality of said comparative circuits, generates an activation signal that activates said clock buffer, and supplies the activation signal to said clock buffer.

18. (Original) The semiconductor integrated circuit according to claim 17, wherein said logic circuit logically synthesizes signals output from a plurality of said comparative circuits into which the same type of signals are input.

19. (Currently Amended) A signal fetching method for fetching an input ~~signals~~ signal in synchronization with an internal clock signal generated by a clock buffer in a semiconductor integrated circuit, comprising:

monitoring if there is a change in said input signal; and

activating said clock buffer [[only]] when the change in said input signal is detected, so that the clock buffer generates said internal clock signal, in synchronization with which the input ~~signals are~~ signal is fetched.

20. (Currently Amended) A signal fetching method for fetching input signals in synchronization with an internal clock signal generated by a clock buffer at a plurality of input buffers in a semiconductor integrated circuit, comprising:

monitoring if there is a change in said input signals respectively supplied to said plurality of input buffers; and

activating said clock buffer when the change in at least one of said input signals supplied to at least one of said input buffers is detected, so that the clock buffer generates said internal clock signal, in synchronization with which the input signals are fetched.

21. (New) The semiconductor integrated circuit according to claim 13, wherein said input signal is selected from the group consisting of a command signal and an address signal.

22. (New) The semiconductor integrated circuit according to claims 15, wherein said input signals are selected from the group consisting of command signals and address signals.

23. (New) The semiconductor integrated circuit according to claims 16, wherein said input signals are selected from the group consisting of command signals and address signals.

24. (New) A semiconductor memory comprising a first input circuit and a second input circuit,

wherein said first input circuit comprising:

a first clock buffer for generating a first internal clock signal;

a first input buffer that fetches a command signal in synchronization with said first internal clock signal provided from said first clock buffer; and

a first clock buffer controller that, upon detecting a change in said command signal, activates said first clock buffer to generate said first internal clock signal and to provide said first internal clock signal to said first input buffer,

and said second input circuit comprising:

a second clock buffer for generating a second internal clock signal;

a second input buffer that fetches an address signal in synchronization with said second internal clock signal provided from said second clock buffer; and

a second clock buffer controller that, upon detecting a change in said address signal, activates said second clock buffer to generate said second internal clock signal and to provide said second internal clock signal to said second input buffer.

25. (New) A semiconductor memory comprising a first input circuit and a second input circuit,

wherein said first input circuit comprising:

a first clock buffer for generating a first internal clock signal;

a plurality of first input buffers that fetches command signals in synchronization with said first internal clock signal generated by said first clock buffer; and

a first clock buffer controller that, upon detecting a change in at least one of said command signals, activates said first clock buffer to generate said first internal clock signal and to provide said first internal clock signal to said plurality of first input buffers,

and said second input circuit comprising:

a second clock buffer for generating a second internal clock signal;

a plurality of second input buffers that fetches address signals in synchronization with said second internal clock signal generated by said second clock buffer; and

a second clock buffer controller that, upon detecting a change in at least one of said address signals, activates said second clock buffer to generate said second internal clock signal and to provide said second internal clock signal to said plurality of second input buffers.

26. (New) A semiconductor memory comprising a first input circuit and a second input circuit,

wherein said first input circuit comprising:

a first clock buffer for generating a first internal clock signal;

a plurality of first input buffers that fetches command signals in synchronization with said first internal clock signal generated by said first clock buffer; and

a plurality of first clock buffer controllers being provided corresponding to each of said first input buffers that, upon detecting a change in said command signal supplied to each corresponding first input buffer, activates said first clock buffer to generate said first internal clock signal and to provide said first internal clock signal to said plurality of first input buffers,

and said second input circuit comprising:

a second clock buffer for generating a second internal clock signal;

a plurality of second input buffers that fetches address signals in synchronization with said second internal clock signal generated by said second clock buffer; and

a plurality of second clock buffer controllers being provided corresponding to each of said second input buffers that, upon detecting a change in said address signal supplied to each corresponding second input buffer, activates said second clock buffer to generate said second internal clock signal and to provide said second internal clock signal to said plurality of second input buffers.